## REMARKS/ARGUMENTS

Independent claims 1, 17 and 22 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Each of these amended claims recites statutory subject matter. As to claim 1, a specific and substantial application is found, as based on a determination made in a processor, a switch is made to a second thread and additional instructions of the first thread are performed and stored in a storage instead of flushing the instructions, providing a useful, tangible and concrete result. Similarly, the apparatus of claim 17 is clearly hardware, namely a processor including a processor pipeline. There is no basis for the contention in the Office Action that such processor pipeline "is not a hardware." Instead, as clearly disclosed in the Specification as filed, a processor includes a pipeline having various components such as described in the example pipeline of FIG. 1 of the Specification. Accordingly, execution of one or more instructions of a first thread while preparing to switch to a second thread without a processor stall provides a tangible, concrete and substantial result. Claim 22' recites patentable subject matter for at least the same reasons.

Pending independent claims 1 and 17 stand rejected under 35 U.S.C. § 102(b) over various references, including U.S. Patent No. 6,049,867 (Eickemeyer), U.S. Patent No. 6,076,157 (Borkenhagen 1) and U.S. Patent No. 6,697,935 (Borkenhagen 2). Applicant respectfully traverses the rejection. In this regard, none of the references alone or in combination teach the subject matter set forth in these independent claims. For example, as to claim 1 none of the cited references teach or suggest determining whether a potential long latency occurs based on whether an instruction hits in a lookup table in an instruction decoder, where the lookup table includes entries corresponding to predetermined conditions. Note with regard to Borkenhagen, it nowhere teaches that an instruction is applied to a lookup table that includes entries corresponding to predetermined conditions. Instead, the cited portions of Borkenhagen nowhere teach or suggest applying an instruction to a lookup table. Instead, all that this portion of Borkenhagen teaches is that a translation lookaside buffer includes virtual-to-real address mappings. However, such mappings are not entries corresponding to predetermined conditions, nor does Borkenhagen anywhere teach or suggest applying an instruction to a lookup table to determine whether execution of the given instruction potentially causes a long latency. Nor do the cited references anywhere teach or suggest executing at least one additional instruction

present in a pipeline and storing a result thereof instead of flushing the instruction while preparing to switch to a second thread.

Independent claim 17 is patentable for at least similar reasons. There is no teaching or suggestion of such execution while preparing to switch to another thread, nor is there any teaching or suggestion of a two pipeline stage delay associated with a feedback signal. Note with regard to Eickemeyer, it nowhere teaches a feedback loop coupled between first and second pipeline stages to provide a feedback signal generated in the second stage back to the first stage. In this regard, the Office Action merely refers to a flowchart of Eickemeyer that discloses passing control from a first thread to a second thread. However, nowhere does this method teach a feedback signal that is generated in a second stage, nor a feedback loop coupled between multiple pipeline stages to provide the feedback signal between the stages. Borkenhagen nowhere teaches or suggests providing the recited feedback signal, as the citation of a flowchart in Borkenhagen nowhere teaches the recited feedback loop coupled between multiple processor pipelines stages, as clearly this software executed flowchart does not teach or suggest such a hardware feedback loop between multiple pipeline stages.

For at least similar reasons, the rejection of claim 22 is also overcome.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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